CLAIMS

1. A semiconductor integrated circuit comprising a memory comprising:

one or more pairs of first structures positioned over a semiconductor substrate, wherein each first structure comprises (a) a plurality of floating gates of memory cells and (b) a first conductive line providing control gates for the memory cells, the control gates in each first structure overlying the floating gates of the first structure;

wherein for each pair of first structures S1, S2, the memory comprises:

a plurality of doped regions in the semiconductor substrate, each doped region providing a source/drain region to a memory cell having floating and control gates in the structure S1 and also providing a source/drain region to a memory cell having floating and control gates in the structure S2; and

a second conductive line formed over the semiconductor substrate, wherein a bottom surface of the second conductive line extends between the first structures S1 and S2 and physically contacts the doped regions which provide the source/drain regions to the memory cells having floating and control gates in the structures S1, S2.

2. The integrated circuit of Claim 1 wherein for each pair of the first structures, the corresponding doped regions are separated from each other by insulation regions recessed into the semiconductor substrate.

3. The integrated circuit of Claim 2 wherein for each pair of the first structures, the top surface of the insulation regions that separate the corresponding doped regions is below the bottom surface of the first conductive lines and wherein the corresponding second conductive line overlies and physically contacts the insulation regions.

4. The integrated circuit of Claim 1 wherein for each pair of the first structures, the bottom surface of the corresponding second conductive line is below the first conductive lines everywhere between the corresponding first structures.

5. The integrated circuit of Claim 1 wherein for each pair (S1, S2) of the first structures, the corresponding second conductive line forms a conductive plug at least partially filling a region between the structures S1, S2.

6. A method for fabricating a semiconductor integrated circuit comprising a memory, the method comprising:

forming one or more pairs of first structures over a semiconductor substrate, wherein each first structure comprises (a) a plurality of floating gates of memory cells and (b) a first conductive line providing control gates for the memory cells, the control gates in each first structure overlying the floating gates of the first structure;

forming first doped regions in the semiconductor substrate, wherein each pair (S1, S2) of the first structures corresponds to a plurality of the first doped regions each of which provides (i) a source/drain region to a memory cell having floating and control gates in the structure S1 and (ii) a source/drain region to a memory cell having floating and control gates in the structure S2;

for each pair (S1, S2), forming a second conductive line over the semiconductor substrate, wherein a bottom surface of the second conductive line extends between the first structures S1 and S2 and physically contacts the first doped regions which provide the source/drain regions to the memory cells having floating and control gates in the structures S1, S2.

7. The method of Claim 6 further comprising forming insulation regions recessed into the semiconductor substrate, wherein for each pair of the first structures, the corresponding first doped regions are separated from each other by the insulation regions.

8. The method of Claim 7 wherein forming the insulation regions comprises etching trenches in the semiconductor substrate and filling the trenches with insulation.

9. The method of Claim 7 wherein the insulation regions are formed before the first doped regions.

10. The method of Claim 6 wherein forming a second conductive line comprises forming a conductive layer and etching the conductive layer to form a conductive plug between each pair of structures (S1, S2).

11. The method of Claim 10 wherein for each pair of structures (S1,S2), the structure S1 has a first sidewall facing the structure S2 and has a second sidewall opposite from the first sidewall, and the structure S2 has a first sidewall facing the structure S1 and a second sidewall opposite from the first sidewall, and the etching of the conductive layer results in a third conductive line being formed from the conductive layer over each of the second sidewalls of the structures S1 and S2.

12. The method of Claim 11 wherein each third conductive line over the second sidewall of a first structure provides select gates for the memory cells having their control and floating gates in the first structure.

13. The method of Claim 12 wherein the conductive layer from which the second and third conductive lines are formed comprises a layer L1 and a layer L2, and forming and etching the conductive layer comprises:

forming the layer L1;

forming a mask over the layer L1, the mask having an opening or openings at a location of the first doped regions;

introducing a dopant into the first doped regions;

removing the mask;

forming the layer L2; and

etching the layers L1 and L2.

14. The method of Claim 13 further comprising etching the layer L1 through the opening or openings in the mask before the mask is removed.

15. The method of Claim 12 further comprising forming gate dielectric for select transistors of the memory cells before forming the layer L1;

wherein the layer L1 covers the gate dielectric when the mask is removed.

16. A method for fabricating a semiconductor integrated circuit comprising a memory array, the method comprising:

forming a first insulating layer over a semiconductor substrate;

forming a first conductive layer over the first insulating layer;

forming a second insulating layer over the first conductive layer;

forming a second conductive layer over the second insulating layer;

patterning the first and second conductive layers and the second insulating layer to form a plurality of first structures each of which comprises:

a plurality of floating gates for a plurality of memory cells, the floating gates being formed from the first conductive layer; and

a conductive line made from the second conductive layer and providing control gates for the memory cells;

forming doped regions in the substrate which provide source/drain regions to memory cells of the memory array, such that each first structure has a first sidewall adjacent to a plurality of the doped regions;

forming a third conductive layer over the first structures;

anisotropically etching the third conductive layer, the etching operation being performed without masking the third conductive layer over the memory array, the etching operation forming, from the third conductive layer:

a spacer over a second sidewall of each first structure;

one or more conductive lines each of which extends between adjacent first sidewalls of two first structures and physically contacts the doped regions to which the adjacent first sidewalls are adjacent;

forming an insulator over the spacers and conductive lines made from the third conductive layer.

17. The method of Claim 16 further comprising forming trenches in the substrate and filling the trenches with an insulator, wherein the doped regions adjacent to first sidewalls of two given first structures are separated from each other by the trenches.

18. The method of Claim 16 wherein the substrate does not provide a conductive path to electrically interconnect doped regions adjacent to first sidewalls of two given first structures.

19. The method of Claim 16 wherein each of said conductive lines formed from the third conductive layer forms a conductive plug at least partially filling a region between the first sidewalls of two first structures.